



[Akanksha Jain](#)

University of Texas at Austin
Advisor: Calvin Lin
Research Interests: Memory systems, Machine learning for systems, Caching, Prefetching



[Diman Zad Tootaghaj](#)

Pennsylvania State University
Advisor: Tom La Porta
Research Interests: Computer network, cloud computing, optimization algorithms, fault tolerance



[Elaheh Sadredini](#)

University of Virginia
Advisor: Kevin Skadron
Research Interests: Near data computing, accelerator design for big data applications, reconfigurable computing



[Fan Chen](#)

Duke University
Advisor: Yiran Chen, Hai "Helen" Li
Research Interests: Computer architecture, Machine learning accelerators, emerging nonvolatile memory technologies



[Hoda Naghibijouybari](#)

University of California, Riverside
Advisor: Nael Abu-Ghazaleh
Research Interests: Architectural Support for Security, GPU Security, Computer Architecture, Heterogeneous Computing



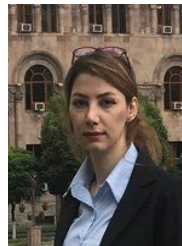
[Itir Akgun](#)

University of California, Santa Barbara
Advisor: Yuan Xie
Research Interests: Computer architecture, interconnects, memory systems, 3D/2.5D integration



[Mao Ye](#)

University of Central Florida
Advisor: Amro Awad
Research Interests: Computer Architecture, Non-volatile Memory



[Masoomesadat Jasemi](#)

University of California, Irvine
Advisor: Nader Bagherzadeh
Research Interests: Machine Learning Accelerators, Memory Design and Architecture based on Conventional and Emerging Technologies, Heterogeneous Architecture



[Nayana Prasad Nagendra](#)

Princeton University
Advisor: David I. August
Research Interests: Computer architecture, microarchitecture design, performance improvement, instruction prefetch, cache management, cloud



[Oana Balmau](#)

University of Sydney
Advisor: Willy Zwaenepoel
Research Interests: Computer Systems, Key-Value Stores, Storage Systems, Data Processing Systems

computing

 <p>Pantea Zardoshti Lehigh University Advisor: Michael Spear Research Interests: Concurrent systems, Compilers, Memory systems, Parallel computing</p>	 <p>Peipei Zhou University of California, Los Angeles Advisor: Jason Cong Research Interests: Reconfigurable Computing, Architecture Modeling, HW/SW Co-design, Deep Learning Accelerator, Energy Efficient Architecture, Cloud Computing, Data Science</p>
<p>Radha Venkatagiri University of Illinois Urbana Champaign Advisor: Sarita Adve Research Interests: Computer Architecture and Systems, Error-Efficient Computing, Hardware Resiliency, Approximate Computing, Software Testing.</p>	<p>Rui Zhang University of North Carolina at Chapel Hill Advisor: Cynthia Sturton Research Interests: Hardware Security, Formal Methods, Computer Architecture</p>
<p>Vijayalakshmi Saravanan Ryerson University, Canada Advisor: Dr. Anpalagan Research Interests: Data science, Big data</p>	<p>Wenjie Xiong Yale University Advisor: Jakub Szefer Research Interests: Hardware security, Computer architecture, cache-based side and covert channels, Physically Unclonable Functions (PUFs)</p>
<p>Xing Hu University of California, Santa Barbara Advisor: Yuan Xie Research Interests: Domain-specific accelerators; machine learning security</p>	

List ordered alphabetically. Please see next few pages for more details/short bio.

**Akanksha Jain**

University of Texas at Austin

Advisor: Calvin Lin

Akanksha Jain is a Research Associate at the University of Texas at Austin. She received her PhD in Computer Science from The University of Texas in December 2016. In 2009, she received the B.Tech and M. Tech degrees in Computer Science and Engineering from the Indian Institute of Technology Madras. Her research interests are in computer architecture, with a particular focus on the memory system and on using machine learning techniques to improve the design of memory system optimizations. Her thesis advances the state-of-the-art for foundational microarchitectural problems, such as cache

replacement and irregular data prefetching. For cache replacement, her work has shown how optimal---but impractical---caching algorithms and prohibitively expensive deep learning algorithms can nonetheless inform the design of practical high-performance replacement policies. For irregular prefetching, her work has shown how better representations of metadata can improve the effectiveness of decades-old ideas in irregular prefetching while dramatically reducing their overhead, making irregular prefetching commercially viable. Her work has won many recognitions including MICRO Best Paper Nominee 2013, Top Picks Honorable Mention 2016, Winner Cache Replacement Championship 2017, Microelectronics and Computer Development Fellowship 2009-2012, Qualcomm Innovation Fellowship Finalist 2016 and MIT EECS Rising Star 2018.

Interested in: Faculty and industry research positions.

Research Interests: Memory systems, Machine learning for systems, Caching, Prefetching

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**Diman Zad Tootaghaj**

The Pennsylvania State University

Advisor: Tom La Porta

Diman Zad-Tootaghaj, is a postdoc/researcher at Hewlett Packard Labs in Palo Alto, California. She works on Software-Defined Network solutions in Wide Area Networks (SD-WAN). She earned her PhD in Computer Science and Engineering at Pennsylvania State University. Prior to Penn State, she got her B.Sc degree in Electrical Engineering at Sharif University of Technology, Iran. During her PhD, she was working in the Institute for Networking and Security Research (INSR) and Network Sciences Research Group (NSRG) under the supervision of Prof. Thomas La Porta (advisor), Dr. Ting He (co-advisor), and Dr.

Novella Bartolini. In her PhD dissertation she explores modeling, monitoring and scheduling techniques for network recovery from massive failures, with a focus on optimization methods under uncertain knowledge of failures.

Interested in: Faculty and industry research positions.

Research Interests: Computer network, cloud computing, optimization algorithms, fault tolerance

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**Elaheh Sadredini**

University of Virginia

Advisor: Kevin Skadron

Elaheh is a postdoctoral researcher at the University of Virginia. She received a Ph.D. degree in Computer Science from the University of Virginia in 2019. Her research interests include accelerator-based, application-specific and reconfigurable architecture, novel computing and memory technologies, and architecture for emerging technologies and applications. Her dissertation work focuses on accelerating complex pattern recognition/matching using memory-centric architectures. The goal of her research is to extract the full compute and storage power from the underlying hardware to provide high-performance,

scalable, flexible, and computationally powerful solutions for complex pattern recognition processing. Elaheh received several research awards including the 2019 John A. Stankovic graduate research award from the Computer Science department of the University of Virginia, ISO graduation award from the University of Virginia in 2019, and two best presentation awards from SRC TECHCON in 2018 and 2019. She also received a best paper award at the ACM International Conference on Computing Frontiers 2016.

Interested in: Faculty, industry research and postdoc positions.

Research Interests: Near data computing, accelerator design for big data applications, reconfigurable computing

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**Fan Chen**

Duke University

Advisor: Yiran Chen, Hai "Helen" Li

Fan Chen is a final-year PhD student in the Department of Electrical and Computer Engineering at Duke University. She is advised by Professor Yiran Chen and Professor Hai "Helen" Li. Her research interests include computer architecture, hardware accelerators for Machine Learning, and emerging nonvolatile memory technologies. Her dissertation investigates these themes as they apply to machine learning applications, demonstrates the challenges of current hardware platforms at both the cloud and at the edge, and discusses how to improve computation and power efficiency with domain-specific

accelerators.

Fan's work has been published in premier computer architecture and EDA conferences, including HPCA, DAC, ICCAD, DATE, ESWEEK, ASP-DAC, GLSVLSI and ISCAS. Fan was awarded Cadence Women in Technology Scholarship in 2019. Her work on the emerging magnetic skyrmions racetrack memory-based cache design received the Best Paper Award at ASP-DAC'18, and her work on accelerator architecture for unsupervised deep learning won the Best Poster Award at ASP-DAC'18.

Interested in: Faculty positions.

Research Interests: Computer architecture, Machine learning accelerators, emerging nonvolatile memory technologies

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**Hoda Naghibijouybari**

University of California, Riverside

Advisor: Nael Abu-Ghazaleh

Hoda Naghibijouybari is a fifth-year Ph.D. Student at UC, Riverside. Her Ph.D. work focuses on Architecture Support for Security and GPU Security. She has demonstrated that the inevitable trend towards sharing on GPUs leads to micro-architectural covert channel and side channel attacks which are substantial threats in GPU-based computational systems including user devices and cloud based systems. She has also proposed architectural mitigations to protect GPU-based systems against these attacks. Her CCS 2018 paper was selected for presentation at Top Picks in Hardware and Embedded Security Workshop (as one of 10, published in 2013-2018 in the area)

Interested in: Faculty and post-doc positions.

Research Interests: Architectural Support for Security, GPU Security, Computer Architecture, Heterogeneous Computing

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**Itir Akgun**

University of California, Santa Barbara

Advisor: Yuan Xie

Itir Akgun is a PhD candidate in the ECE department at the University of California, Santa Barbara, where she is advised by Professor Yuan Xie. She received her MS in ECE from UC Santa Barbara in 2015, and her BS in ECE from University of Illinois at Urbana-Champaign in 2014. During her PhD, she interned at AMD Research and HP Labs. Her PhD work focuses on scalable interconnect architecture design for emerging integration and memory technologies. Specifically, she explores the design space, identifies trade-offs, and proposes scalable solutions for the interconnect architecture design in systems with memory networks, silicon interposers,

and monolithic 3D integration. She is also interested in cost analysis of vertical and interposer stacking systems, exascale system architectures, and domain-specific acceleration of data-intensive applications.

Interested in: Industry research and product positions.

Research Interests: Computer Architecture, Interconnects, Memory Systems and 3D/2.5D Integration

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**Mao Ye**

University of Central Florida

Advisor: Amro Awad

Mao Ye got her Computer Science Master's degree from UCF. Her research interests are non-volatile memory systems, file systems, security and reliability. She got her bachelor's degree from Zhejiang University. Before she started her PhD, she worked several years in an open system department of a national bank in China. She also holds a master's degree in biochemistry and molecular genetics from the University of Pittsburgh.

Interested in: Faculty, industry research and postdoc positions.

Research Interests: Computer Architecture, Non-volatile memory, Memory, security, resilience and reliability

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**Masoomehsadat Jasemi**

University of California, Irvine

Advisor: Nader Bagherzadeh

Masoomehsadat Jasemi is a research scholar in EECS department of University of California Irvine. She is a PhD. Candidate at Sharif University of Technology in Iran. She plans to defend in January 2020 and is actively seeking a full-time position in 2020. She is looking for full-time opportunities as a hardware engineer, software engineer, or research engineer related to computer architecture and accelerator based designs. Her research focuses on mitigating the memory bottleneck of CNN accelerators. With the growing size and complexity of CNNs, the demand for larger on-chip memory increases with each generation.

She has chosen two directions to combat the issues associated with memory in CNN accelerators; 1) Addressing the reliability concerns of NVM-based CNN Accelerators and 2) Reducing the memory footprint through compression of CNN parameters in on-chip memory. NVMs introduce tradeoffs between reliability and on-chip memory size. She proposed two solutions to address these problems. One deals with representation Reformation and the other one trades accuracy for better memory management.

Interested in: Industry research or product, and post-doc positions.

Research Interests: Machine Learning Accelerators, Memory Design and Architecture based on Conventional and Emerging Technologies, Heterogeneous Architecture

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**Nayana Prasad Nagendra**

Princeton University

Advisor: David I. August

Nayana is a final year Ph.D. candidate at Princeton University, advised by Prof. David August. Her research interests are in the field of computer architecture, microarchitecture design, and hardware/software co-design. Her Ph.D. dissertation is focussed on performance improvement at the scale of a Warehouse-Scale Computer. She has interned for two consecutive summers with the Google Wide Profiling team at Google where she identified the root causes for Google's Datacenter performance bottlenecks. Some of the software-level fixes that she provided helped in improving the

performance of live Datacenter applications by nearly 1%, saving millions of dollars in cost and energy. Her thesis work focuses on a hardware-based instruction prefetching technique to reduce instruction cache misses and improve CPU performance, especially at the scale of a Datacenter. Nayana's Ph.D. dissertation provides a simple, efficient instruction prefetching solution to reduce the front-end stalls among the ever growing Datacenter workloads. Before joining Princeton, Nayana was working as a Verification Engineer at AMD, Bangalore, India. Prior to AMD, she earned her Master's degree in Embedded Systems Engineering from the University of Leeds, U.K. in 2010.

Interested in: Industry research positions.**Research Interests:** Computer architecture, microarchitecture design, performance improvement, instruction prefetch, cache management, cloud computing**Email:** nagendra@princeton.edu**Web:** <https://www.cs.princeton.edu/~nagendra/>

Oana Balmau

University of Sydney

Advisor: Willy Zwaenepoel

Oana Balmau is a PhD student at the University of Sydney, advised by Prof. Willy Zwaenepoel. She completed her Bachelor and Master studies in Computer Science at EPFL, Switzerland. Her research focuses on Computer Systems, Storage and Concurrency, with an emphasis on optimizations for key-value stores. During her PhD, she has worked on persistent key-value stores, designing techniques to reduce write amplification on SSDs [USENIX ATC '17], to improve scalability with memory size and the number of threads [EuroSys '17], to prevent tail latency spikes [USENIX ATC '19 - Best Paper Award], and to take advantage of new fast drives (e.g., Intel

Optane NVMe SSDs) [SOSP '19]. She has received multiple recognitions including EPFL Fellowship for Doctoral Students and University of Sydney Faculty of Engineering Dean's Postgraduate Research Scholarship.

Interested in: Faculty and industry research positions.

Research Interests: Computer Systems, Key-Value Stores, Storage Systems, Data Processing Systems

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**Pantea Zardoshti**

Lehigh University

Advisor: Michael Spear

Pantea Zardoshti is a fourth year PhD student at Lehigh University in CSE department working on hardware/software co-design for emerging memory technologies and compiler support for Abstract Instrumented Memory Interfaces, which allow programmers to exploit hardware and software memory features. Her previous work focused on adaptive sparse matrix representations for efficient matrix-vector multiplication on GPUs. Pantea obtained her B.Sc. and M.Sc. in computer engineering with the highest honor and joined the Institute for Research in Fundamental Science (IPM) as a research

assistant. In Iran, she received the silver medal in the National Computer Science Olympiad and an Outstanding Student Award. Her work has also been recognized with several awards such as the CRA-W Scholarship in 2017, the GHC Scholarship in 2018, the ACM travel award both in 2018 and 2019, the NSF travel award in 2018. Her work was ranked 109 in the Nationwide Examination for Undergraduate Admissions in the Public Universities in Iran in 2005. She was also recognised with the best Iranian Student Award from the National Organization for Development of Exceptional Talents in Iran in 2004.

Interested in: Industry research or product positions.

Research Interests: Concurrent systems, Compilers, Memory systems, Parallel computing

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**Peipei Zhou**

University of California, Los Angeles

Advisor: Jason Cong

Peipei Zhou is a research scientist in Shanghai Enflame Technology (AI Chip Startup). She received her Ph.D. in Computer Science from the University of California, Los Angeles in 2019. In 2012, she received a B.S. in Electrical Engineering from Chien-Shiung Wu Honors College, Southeast University. Her Ph.D. thesis investigates design targets, modeling, and optimization for field-programmable gate array (FPGA) customized computing at three levels including chip-level, node-level and cluster-level. Her research work advances modeling and optimization of FPGA based reconfigurable architecture from

performance, energy, and cost perspective for applications including deep learning, precision medicine and other big-data and machine learning applications.

She has in total 9 papers published in FCCM, ISPASS, DAC, ICCAD, TCAD with 4 first authored paper. She has won 2019 IEEE Donald O. Pederson Best Paper Award (TCAD Best Paper), 2019 UCLA CS Outstanding Researcher Award, 2018 ICCAD Best Paper Nominee, 2018 ISPASS Best Paper Nominee, 2018 Phi Tau Phi Scholarship, 2018 DAC PhD Travel Grant. She is passionate in computer architecture research and teaching.

Interested in: Faculty positions.

Research Interests: Reconfigurable Computing, Architecture Modeling, HW/SW Co-design, Deep Learning Accelerator, Energy Efficient Architecture, Cloud Computing, Data Science

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Radha Venkatagiri

University of Illinois at Urbana Champaign

Advisor: Sarita Adve

Radha is a doctoral candidate in Computer Science at the University of Illinois at Urbana-Champaign. Her research interests lie in the area of Computer Architecture and Systems. Radha's dissertation work aims to build efficient computing systems that redefine "correctness" as producing results that are good enough to ensure an acceptable user experience. Radha's research work has been published in the top Computer Architecture and Dependability conferences (ISCA, MICRO, ASPLOS, DSN). Her work has been nominated to the IBM Pat Goldberg Memorial Best Paper Award for 2019. She was among 20 people

invited to participate in an exploratory workshop on error-efficient computing systems initiated by the Swiss National Science Foundation and is one of 200 young researchers in Math and Computer Science worldwide to be selected for the prestigious 2018 Heidelberg Laureate Forum. Radha was selected for the Rising Stars in EECS and the Rising Stars in Computer Architecture (RISC-A) workshops for the year 2019. Before joining the University of Illinois, Radha was a CPU/Silicon validation engineer at Intel where her work won a divisional award for key contributions in validating new industry standard CPU features. Prior to that, she worked briefly at Qualcomm on architectural verification of the Snapdragon processor.

Interested in: Faculty and industry research positions.

Research Interests: Computer Architecture and Systems, Error-Efficient Computing, Hardware Resiliency, Approximate Computing, Software Testing.

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Rui Zhang

University of North Carolina at Chapel Hill

Advisor: Cynthia Sturton

Rui Zhang is a PhD candidate in the Computer Science Department at University of North Carolina at Chapel Hill. She is advised by Professor Cynthia Sturton. Her research interests lie at the intersection of formal analysis techniques and hardware security. Her work designs formal, automated systems and tools for generating and translating hardware security property, detecting vulnerabilities and validating the security of hardware designs. Her research has been recognized with a best paper award nomination at MICRO 2018. Rui was selected for 2019 Rising Stars in EECS Workshop; selected for the second Rising

Stars in Computer Architecture Workshop; and selected for the seventh Heidelberg Laureate Forum. She was also nominated as one of two candidates for Google PhD fellowship representing UNC Chapel Hill in 2016. She received her master's degree from Columbia University in 2015 and her bachelor's degree from Peking University in 2013.

Interested in: Faculty and industry research positions.

Research Interests: Hardware Security, Formal Methods and Computer Architecture

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Vijayalakshmi Saravanan

Ryerson University, Canada

Advisor: Dr. Anpalagan

Vijayalakshmi Saravanan received her Ph.D. in Computer Science and Engineering from VIT University, India under Erasmus Mundus Fellowship (EURECA) as a research exchange student at Mälardalen University, Sweden, and is currently an Adjunct Faculty at Rochester Institute of Technology, USA. She was working as an Assistant Professor in Practice at the University of Texas, San Antonio (UTSA) in the Department of Computer Science. Prior to this, she was a Postdoctoral Associate at UB (University at Buffalo), The State University of New York, USA and University of Waterloo, Canada

under the prestigious “Schlumberger Faculty for the Future” Fellowship award (2015-2017). She has 10 years of teaching experience in two premier universities: VIT and Amrita Vishwa Vidyapeetham, India. Dr. Saravanan has published many technical articles in scholarly international journal and conferences. She is serving as a technical reviewer and program committee member for reputed conference & journals such as GHC, SIGCSE, and Springer. Her research interests include Power-Aware Processor Design, Big Data, IoT and Computer Architecture. She is a Senior Member of IEEE & ACM, CSI, Ex-Chair for IEEE-WIE VIT affinity group, India (2009-2015), NPA (National Postdoctoral Association) Annual Meetings committee, Workshop/IIA Co-Chair (2017-2018) and a Board member of N2WOMEN (Networking Networking Women).

Interested in: Faculty and industry research positions.

Research Interests: Data science, Big data

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Wenjie Xiong

Yale University

Advisor: Jakub Szefer

Wenjie Xiong is a final-year Ph.D. student in the Department of Electrical Engineering at Yale University, advised by Prof. Jakub Szefer. She received her B.S. degrees in Microelectronics and Psychology from Peking University and her M.S. degree in Electrical Engineering from Yale University. She works on hardware security. She proposed run-time DRAM Physically Unclonable Functions (PUFs) for device authentication, key storage, and software protection. She also explores new cache timing channels and their formal models. Her dissertation research shows how DRAM can be leveraged as physically unclonable

functions (PUFs) for device authentication, key storage, and software protection. Her dissertation also includes a new covert channel in the processor cache states. She was awarded Microsoft Research Graduate Women's Scholars in 2015 and selected as a participant in the third Heidelberg Laureate Forum. Her work on run-time accessible DRAM PUFs was selected as a candidate for Top Picks in Hardware and Embedded Security 2019. Her work titled "Intrinsic Rowhammer PUFs: Leveraging the Rowhammer effect for improved security" was selected as Best Student Paper Finalist in HOST 2017.

Interested in: Industry research and postdoc positions.

Research Interests: Hardware security, Computer architecture, cache-based side and covert channels, Physically Unclonable Functions (PUFs)

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Xing Hu

University of California, Santa Barbara

Advisor: Yuan Xie

Xing Hu is a postdoc in the SEALab, Dept. of ECE, UCSB since Jan. 2017. She received her Ph. D. degree from the Institute of Computing Technology (ICT), Chinese Academy of Sciences (CAS). Her research interests include in-memory-computing architectures for domain-specific applications.

Interested in: Faculty and industry research positions.

Research Interests: Domain-specific accelerators; machine learning security

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