Rank	Citations	Year	Title (★ means it won the ISCA Influential Paper Award)	First Author + HOF Authors	Type	Topic
1	5351	1995	The SPLASH-2 programs: Characterization and methodological considerations	Stephen Woo, *Anoop Gupta*	Tool	Benchmark
2	4214	2017	In-datacenter performance analysis of a Tensor Processing Unit	*Norm Jouppi, David Patterson*	Arch	Machine Learning
3	3834	2000	★ Wattch: A framework for architectural-level power analysis and optimizations	*David Brooks, Margaret Martonosi*	Tool	Power
4	3386	1993	★ Transactional memory: Architectural support for lock-free data structures	Maurice Herlihy	Micro	Parallelism
5	2690	2016	EIE: Efficient inference engine on compressed deep neural network	Song Han, *Bill Dally, Mark Horowitz*	Arch	Machine Learning
6	2620	2007	★ Power provisioning for a warehouse-sized computer	Xiaobo Fan, *Luiz Barroso*	Micro	Power
7	2507	1992	Active messages: a mechanism for integrated communication and computation	Thorsten von Eiken	Micro	Parallelism
8	2391	2011	Dark silicon and the end of multicore scaling	*Hadi Esmaeilzadeh, Doug Burger, Karthikeyan Sankaralingam*	Micro	Parallelism
9	2352	1995	★ Simultaneous multithreading: Maximizing on-chip parallelism	*Dean Tullsen, Susan Eggers, Hank Levy*	Micro	Parallelism
10	2243	1990	★ Improving direct-mapped cache performance by the addition of a small fully-associative cache and prefetch buffers	*Norm Jouppi*	Micro	Cache
11	1801	2009	Architecting phase change memory as a scalable DRAM Alternative	Benjamin Lee, *Doug Burger, Engin Ipek, Onur Mutlu*	Micro	NV RAM
12	1790	1990	Memory consistency and event ordering in scalable shared-memory multiprocessors	*Kourosh Gharachorloo, Anoop Gupta, John Hennessy*	Micro	Consistency/ Coherence
13	1769	2009	Scalable high performance main memory system using phase-change memory technology	*Moinuddin Qureshi*	Micro	NV RAM
14	1659	2016	ISAAC: A convolutional neural network accelerator with in-situ analog arithmetic in crossbars	Ali Shafiee, *Rajeev Balasubramonian, Naveen Muralimanohar*	Arch	Machine Learning
15	1643	2003	★ Temperature-aware microarchitecture	Kevin Skandron	Micro	Power
16	1557	2016	Eyeriss: A spatial architecture for energy-efficient dataflow for convolutional neural networks	Yu-Hsin Chen, *Joel Emer*	Micro	Machine Learning
17	1420	2016	Prime: A novel processing-in-memory architecture for neural network computation in ReRAM-based main memory	Ping Chi, *Yuan Xie*	Arch	Machine Learning
18	1401	2014	A reconfigurable fabric for accelerating large-scale datacenter services	Andrew Putnam, *Hadi Esmaeilzadeh*	Micro	Interconnect
19	1374	1992	The turn model for adaptive routing	Christopher Glass	Micro	Interconnect
20	1350	1995	Multiscalar processors	*Guri Sohi, T. N. Vijaykumar*	Micro	Parallelism
21	1302	2000	Memory access scheduling	Andrew Putnam, *Bill Dally*	Micro	Parallelism
22	1284	1997	★ Complexity-effective superscalar processors	Subbarao Palacharla, *Norm Jouppi, Jim Smith*	Micro	Parallelism
23	1221	2002	★ Drowsy caches: simple techniques for reducing leakage power	Krisztián Flautner, *Nam Sung Kim, Trevor Mudge*	Micro	Power
24	1210	1996	★ Exploiting choice: Instruction fetch and issue on an implementable simultaneous multithreading processor	*Hank Levy, Susan Eggers, Joel Emer, Dean Tullsen*	Micro	Parallelism
25	1201	1997	A Study of Branch Prediction Strategies	*Jim Smith*	Micro	Parallelism