Rank	Citations	Year	Title (★ means it won the ISCA Influential Paper Award)	First Author + HOF Authors	Type	Topic
26	1201	1997	The SGI Origin: A ccNUMA highly scalable server	James Laudon	Arch	Consistency/ Coherence
27	1177	2009	A durable and energy efficient main memory using phase change memory technology	Ping Zhou	Tool	Benchmark
28	1175	2014	Flipping bits in memory without accessing them: An experimental study of DRAM disturbance errors	Yoongu Kim, *Onur Mutlu, Chris Wilkerson*	Micro	Security
29	1166	2010	Debunking the 100X GPU vs. CPU myth: an evaluation of throughput computing on CPU and GPU	Victor Lee	Tool	Simulator
30	1104	2017	SCNN: An accelerator for compressed-sparse convolutional neural networks	Angshuman Parashar, *Joel Emer, Bill Dally, Steve Keckler*	Arch	Machine Learning
31	1070	2015	ShiDianNao: Shifting vision processing closer to the sensor	Zidong Du	Arch	Machine Learning
32	1051	1994	★ The Stanford FLASH multiprocessor	Jeffrey Kuskin, *Kourosh Gharachorloo, Anoop Gupta, John Hennessy, Mark Horowitz*	Arch	Parallelism
33	1027	2004	★ Transactional memory coherence and consistency	Lance Hammond, *Christos Kozyrakis, Kunle Olukotun*	Micro	Consistency/ Coherence
34	1021	1992	Lazy release consistency for software distributed shared memory	Pete Keleher	Micro	Consistency/ Coherence
35	1006	2001	Cache decay: Exploiting generational behavior to reduce cache leakage power	*Stefanos Kaxiras, Margaret Martonosi*	Micro	Power
36	993	1990	The directory-based cache coherence protocol for the DASH multiprocessor	Daniel Lenoski, *Kourosh Gharachorloo, Anoop Gupta, John Hennessy*	Micro	Consistency/ Coherence
37	991	2000	Clock rate versus IPC: The end of the road for conventional microarchitectures	Vikas Agarwal, *Doug Burger, Steve Keckler*	Micro	Parallelism
38	980	1990	Weak ordering—a new definition	*Sarita Adve, Mark Hill*	Micro	Consistency/ Coherence
39	957	2008	Technology-driven, highly-scalable dragonfly topology	*John Kim, Bill Dally*	Micro	Interconnect
40	938	2007	Adaptive insertion policies for high performance caching	*Moinuddin Qureshi, Joel Emer, Yale Patt*	Micro	Cache
41	935	1973	Banyan networks for partitioning multiprocessor systems	Rodney Goke, *Jack Lipovski*	Micro	Interconnect
42	911	2008	3D-Stacked Memory Architectures for Multi-core Processors	*Gabriel Loh*	Micro	Cache
43	895	2010	High performance cache replacement using re-reference interval prediction (RRIP)	*Aamer Jaleel, Joel Emer*	Micro	Cache
44	877	2015	A scalable processing-in-memory accelerator for parallel graph processing	Junwhan Ahn, *Onur Mutlu*	Arch	Parallelism
45	873	2000	Transient fault detection via simultaneous multithreading	*Steven Reinhardt*	Micro	Reliability
46	868	2008	Corona: System implications of emerging nanophotonic technology	Dana Vantrease, *Norm Jouppi*	Micro	Interconnect
47	863	2009	An analytical model for a GPU architecture with memory-level and thread-level parallelism awareness	Sunpyo Hong	Tool	Parallelism
48	859	2004	Single-ISA heterogeneous multi-core architectures for multithreaded workload performance	*Rakesh Kumar, Norm Jouppi, Partha Ranganathan & Dean Tullsen*	Micro	Parallelism
49	854	1974	A Preliminary Architecture for a Basic Data Flow Processor	Jack Dennis	Arch	Parallelism
50	854	1983	Very Long Instruction Word Architectures and the ELI-512	Josh Fisher	Arch	Parallelism